



JCT1231C 30

FIG.1 Maximum power dissipation versus RMS on-state current

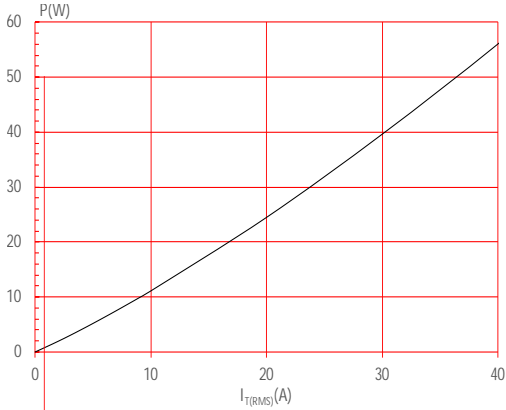


FIG.3: Surge peak on-state current versus number of cycles

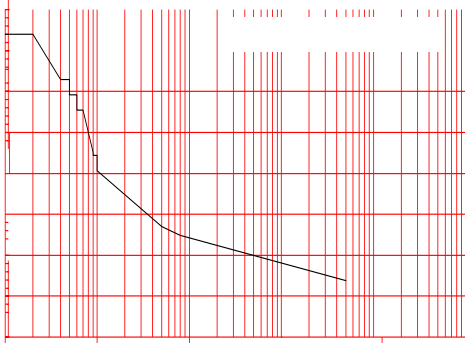


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10\text{ms}$, and corresponding value of I^2t ($di/dt < 200\text{A}/\mu\text{s}$)

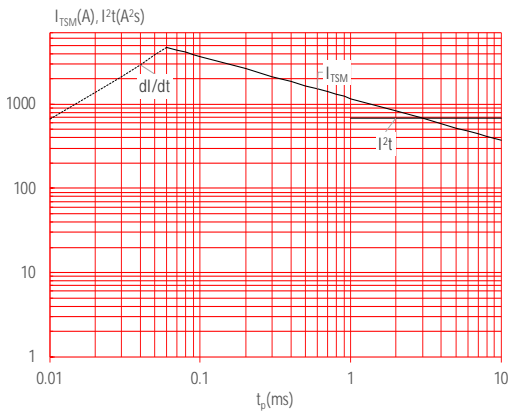


FIG.2: RMS on-state current versus case temperature

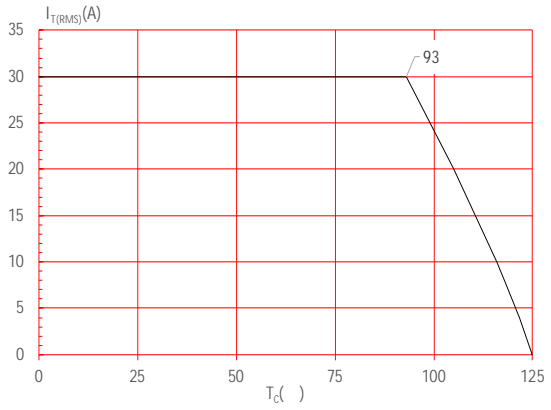


FIG.4: On-state characteristics

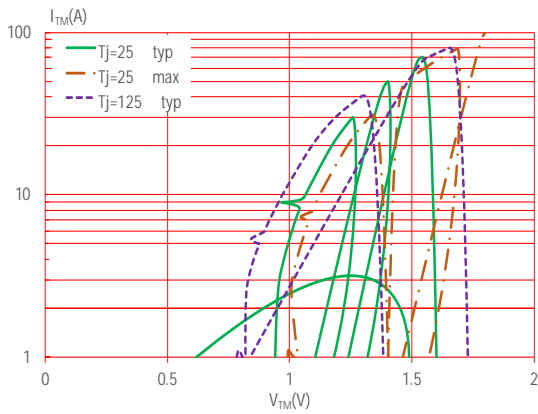


FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature

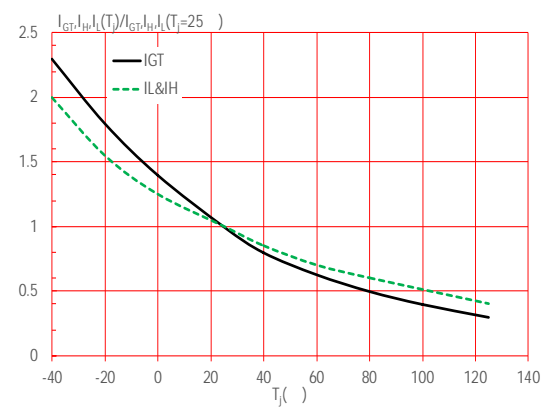
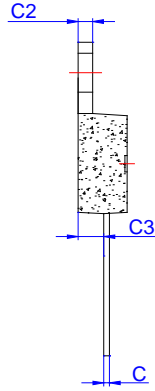
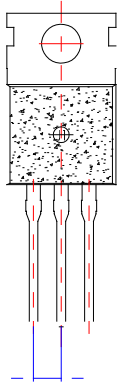
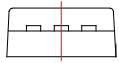


FIG.7: Test circuit for inductive and resistive loads to IEC


| Order code | Voltage V_{DRM}/V_{RRM} (V) | IGT(mA) | Package | Base qty. (pcs) | Delivery mode |
|------------|----------------------------------|---------|---------|--------------------|------------------|
| JCT1231C | 1200 | 40 | TO-220C | 50 | Tube |

Document Revision History

| Date | Revision | Changes |
|--------------|----------|-------------|
| Apr.13, 2023 | A.1.0 | Last update |



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